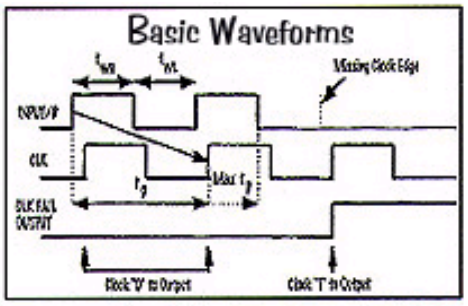
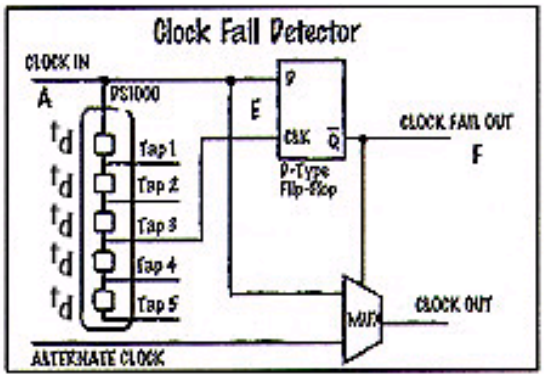
Spare Gates and Unused Delay Lines Can be Used to Build a Clock Fail Detection Circuit

A common design need is to detect the presence or absence of a clock signal. In the absence of a clock, it may be necessary to switch to an alternate reference or at least notify the system that a failure has occurred. A delay can be used to anticipate when a clock edge is due and initiate a sample of the input waveform to verify that the pulse is present.



The circuitry is surprisingly simple, adding only a flip-flop to the delay line itself. Adding a simple multiplexer or a few gates allows automatic switching to an alternate clock source.

The required delay time (t_D) must be in the range from greater than one full clock period to less than 1.5 clock periods. Obviously, the minimum acceptable delay for correct operation will be when the delay is longer than one clock period, allowing adequate safety margin for the rise time of the clock edge. The maximum acceptable delay will be 1.5 times the input period minus the hold time of the flip-flop, since the sample must be taken before the next high-to-low transition of the input clock.



A multitap delay must be used because the time from the first rising edge of the clock to the sampling point (t_D) is slightly more than one full clock period (t_{WH} + t_{WL}). Since the "minimum input pulse width" specification restricts us to one-half period delay maximum, the simple solution is to break down the delay into three smaller increments, such as is provided in a multitap device.

In Equations:

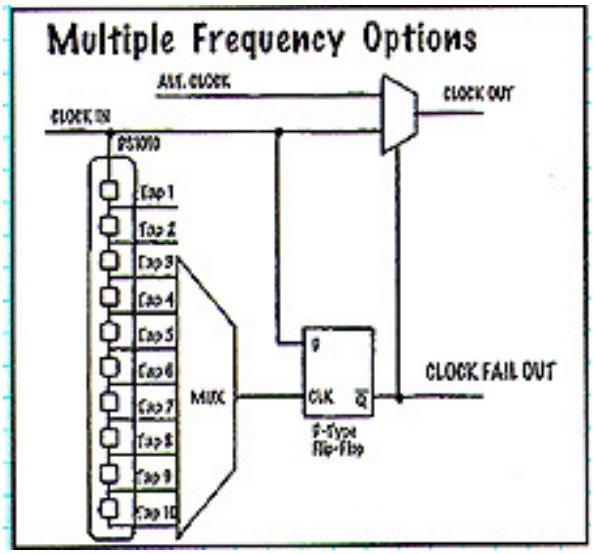
$t_{WH} + t_{WL} < t_D < 2t_{WH} + t_{WL}$ *(Application constraint)*
$t_d < t_{WI}$ **(lower of** t_{WH} **or** t_{WL}**)** *(Device constraint)*
therefore: $t_D > 2t_d$ *(for 50% duty cycle,* $t_{WH} = t_{WL}$*)*

where t_d ***is the delay time of a single tap.***

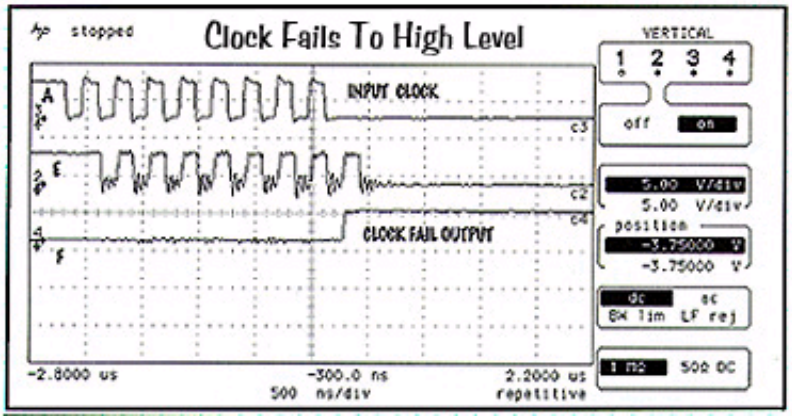
Three taps is therefore a good choice with a 50/50 input clock; however, more stages may be needed if the clock is very asymmetrical.

In all cases, the output flag will be set within half a clock period of the missing edge (plus the propagation delay of the flip-flop itself). When the clock is restored, there will be a latency period equal to the delay time before the flip-flop is reset.

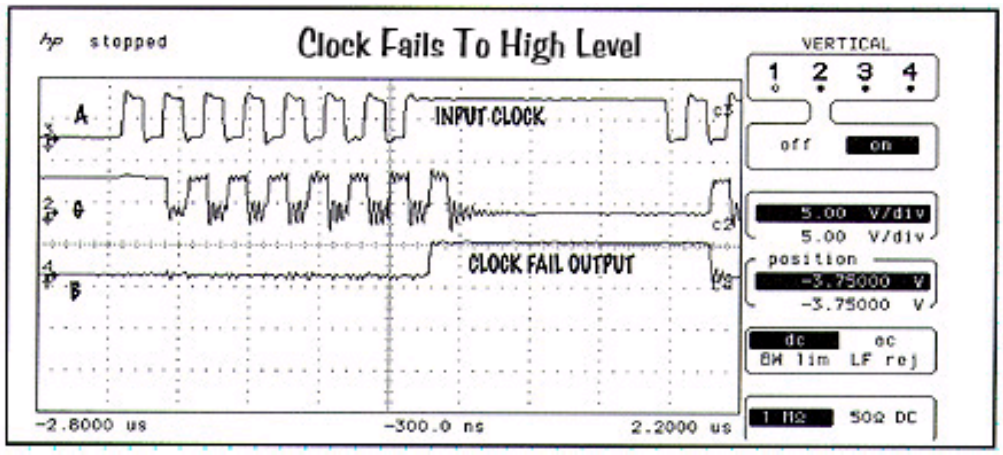
It is even possible to increase the complexity to allow for several different clock frequencies. Simply add more taps and use a mux (adding its propagation delay too) or hardwire and reroute the appropriate tap into the clock input of the flip-flop.



These examples assume that the clock input reverts to a low level when the clock fails. The corresponding waveforms can be seen in the diagram.



If the clock fails high, an inverter on the CLK input of the flip-flop and the use of the Q rather than the Q\ output can be used instead. The resulting waveforms can be seen in the diagram.



If the clock can fail to either state, a combination circuit can be used as shown.